Display Port Adapters
PLIP Level II training in Shenzhen

David Li  David.j.li@NXP.com
NXP Semiconductors

June, 2010
NXP enables DisplayPort
Contents

- NXP’s DisplayPort-VGA Adapter PTN3392
  - Our Value Propositions
  - BOM Cost
  - DPVGA4 and DPVGA4M Reference Dongle Designs
  - Summary Test Results

- NXP’s DisplayPort Roadmap
  - Next: PTN3372 is the same as PTN3392, and includes 5V regulator to achieve even lower system BOM
  - Low-Power DisplayPort-VGA Adapter PTN3352

- NXP’s DisplayPort-DVI and DisplayPort-HDMI solutions

- Appendices for PTN3392
  - Firmware Update via Host: Flash over AUX
  - Compliance, Interop, EMI, ESD Tests Results
# NXP DisplayPort Adapter Products

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTN3360A, PTN3360B</td>
<td>Production</td>
</tr>
<tr>
<td>Enhanced DisplayPort-DVI/HDMI Level Shifters (Follow-up versions of PTN3300A, PTN3300B)</td>
<td></td>
</tr>
<tr>
<td>PTN3361B</td>
<td>Production</td>
</tr>
<tr>
<td>Enhanced DisplayPort-DVI/HDMI Level Shifters w/ DDC buffer, feature optimized for dongle application</td>
<td></td>
</tr>
<tr>
<td>PTN3380B</td>
<td>Production</td>
</tr>
<tr>
<td>Enhanced DisplayPort-DVI/HDMI Level Shifters w/ 5V voltage regulator, cost and feature optimized for dongle application</td>
<td></td>
</tr>
<tr>
<td>PTN3381B</td>
<td>Sampling Now</td>
</tr>
<tr>
<td>Enhanced DisplayPort-DVI/HDMI Level Shifters w/ DDC buffer and 5V voltage regulator, cost and feature optimized for dongle application</td>
<td></td>
</tr>
<tr>
<td>PTN3360D</td>
<td>Production</td>
</tr>
<tr>
<td>Enhanced DisplayPort-HDMI Level Shifter with Deep Color Support for HDMI on Motherboard</td>
<td></td>
</tr>
<tr>
<td>PTN3392</td>
<td>Production</td>
</tr>
<tr>
<td>2-lane DisplayPort-to-VGA Adaptor IC, cost and feature optimized for VGA dongle</td>
<td></td>
</tr>
<tr>
<td>PTN3372</td>
<td>Sampling Now</td>
</tr>
<tr>
<td>2-lane DisplayPort-to-VGA Adaptor IC, w/ 5V voltage regulator, cost and feature optimized for VGA dongle</td>
<td></td>
</tr>
</tbody>
</table>
PTN3392 - DisplayPort to VGA Bridge

- DisplayPort receiver v1.1a
  - 1-lane / 2-lane 2.7Gb/s / 1.62Gb/s
  - AUX channel, HPD support

- Output
  - Analog RGB, HSYNC, VSYNC
  - Up to 240MHz, 8bits color
  - DDC

- Resolutions
  - WUXGA: 1920 x 1200, 60Hz, 193MHz clock
  - UXGA: 1600 x 1200, 60Hz, 162MHz clock
  - SXGA (CRT): 1280 x 1024, 80Hz, 135MHz clock
  - SXGA: 1280 x 1024, 60Hz, 108MHz clock
  - XGA: 1024 x 768, 60Hz, 65MHz clock
  - VGA: 640 x 480, 60Hz, 25MHz clock

- AUX channel to I²C DDC channel bridge

- Supports Flash over AUX field upgradability

- Use only power from DP connector 3.3V

- < 610mW Active @ 1920 x 1200; 150mW Standby; 500mW Init

- No support for HDCP and audio

- HVQFN48, 7x7mm, 0.5mm pitch

- ESD 7kV HBM

In Production
PTN3392 Block Diagram
NXP’s DisplayPort-VGA Dongle

- PTN3392 has Embedded Flash
  - PTN3392 DisplayPort-VGA Adapter
  - 27 MHz crystal
  - 3.3V-to-5V regulator
  - No Need For
    - External flash
    - 3.3V-to-1.2V LDO
    - External ESD protection
  - PTN3372 integrates 3.3V-to-5V regulator

- Pros
  - Industry’s lowest component count and BOM
  - Enable small-size dongle with smallest package and low BOM
  - Monitor detect by load sensing allows DP source; Support power saving upon monitor detachment
  - Flash programming over AUX CH, enabling future firmware driver download from the host

- Interoperability
  - MacBook Pro/ NVIDIA 9400M / 9600GT
  - Windows / Dell Latitude E5400 / Intel GMA4500
  - Windows / Dell Latitude E6500 / NVIDIA Quadro NVS160M
  - Windows / Dell Studio 1440 / NVIDIA Quadro FX2700
  - Windows / ATI Radeon HD5750 GPU Card
  - Windows / HP ProBook 5310m / Intel GMA 4500

Good interoperability
PTN3392 Bill of Materials

- Industry’s Lowest System BOM
  - PTN3392
  - 27 MHz crystal
  - 3.3V-to-5V regulator
  - Filter for VGA

- No Need For
  - External flash
  - 3.3V-to-1.2V LDO
PTN3392 Firmware Update Via the Host AUX CH

- Interoperability issues due to …
  - “Holes” in DP specification and interoperability guidelines document
  - Differences in spec interpretation between DP TX and RX vendors
  - Workaround solutions
  - Insufficient regression testing of DP source driver updates

- Value Proposition of Flash Programming over AUX CH
  - Uses host computer to download firmware fix or upgrade to dongle
  - Without additional hardware
  - NXP will host a web site for dongle end users to download various dongle firmware versions

- Implementation depends on availability of SDK from GPU vendors allowing the feature
  - NVIDIA / Windows  NXP’s implementation ready
  - AMD / Windows    NXP’s implementation ready
  - Intel / Windows   NXP’s implementation ready
DPVGA4

NXP DP-VGA reference design dongle with PTN3392 and PTN3372

- Availability: NOW
- Reference Dongle Design
  - Uses PTN3392 or PTN3372 (stuff option)
  - Form factor close to a real dongle (but with still some debug capabilities)
  - Reflects best practices in schematics & layout
  - Reflects best-in-class BOM cost
  - Optimized for EMI
  - Optimized for VSIS performance
  - Purity of signals, reference planes
  - Final PTN3392 reference design schematic and BOM
  - Minimized size
  - Optimized component cost / quality
  - No external ESD protection needed for passing IEC ESD tests

- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC

- Purposes
  1. Customer reference design
  2. PTN3392 interop testing
  3. Trade show demos
DPVGA4M

NXP DP-VGA reference design dongle with PTN3392 and PTN3372
Complete with plastic encasing

- Availability: NOW

- Reference Dongle Design
  - Uses PTN3392 or PTN3372 (stuff option)
  - Production-ready form factor
  - Reflects best practices in schematics & layout
  - Reflects best-in-class BOM cost
  - Optimized for EMI
  - Optimized for VSIS performance
  - Purity of signals, reference planes
  - Final PTN3392 reference design schematic and BOM
  - Minimized size
  - Optimized component cost / quality
  - No external ESD protection needed for passing IEC ESD tests

- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC
PTN3392 Test Status Summary

- DisplayPort v1.1a PHY-Layer Compliance Tests
  - Spec: VESA DisplayPort PHY CTS 1.1 or latest governing specification
  - Setup: Tektronix AWG Compliance Test Suite
  - Conditions: RBR & HBR, across supply voltage and temperature
  - Status: ALL PASS

- DisplayPort v1.1a Link-Layer Compliance Tests
  - Spec: VESA DisplayPort LLC CTS 1.1a or latest governing specification
  - Setup: Quantum Data DisplayPort Link-Layer Analyzer
  - Status: ALL PASS

- DisplayPort AUX CH Compliance Tests (Preliminary Results at Yokohama VESA Plugtest Dec 2009)
  - Status: PASS

- Inrush Current Tests
  - Status: PASS

- VSIS 1.2 Compliance Tests
  - Spec: VESA VSIS v1.r2
  - Setup: Tektronix VM6000 VSIS Compliance Test Suite
  - Conditions: 800 x 600, 60Hz, DMT, 40MHz ; 800 x 600, 85Hz, DMT, 56MHz ; 1024 x 768, 75Hz, DMT, 81MHz ; 1600 x 1200, 65Hz, DMT, 175MHz
  - Status: PASS
  - DPVGA4 board - Final BOM optimization is in progress

- EMI Tests
  - Spec: CISPR22B
  - Setup: EMI chamber test
  - Status: PASS without metal shielding, but without the needed 3-6dB margin
  - Recommend use of metal tape around VGA connector or use of metal can to pass EMI tests with sufficient margin

- ESD Tests
  - Spec: IEC61000-4-2 8 kV contact discharge, 15 kV air discharge
  - Setup: Only applicable on over-molded version of dongle
  - Status: PASS without external ESD protection
PTN3392 Order Entry Options

PTN3392BS

- BS = HVQFN48 plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; 7x7x0.85 mm SOT619-1
- “Trust NXP” option – automatic firmware upgrades
- Backward compatible firmware
- Customer automatically gets latest firmware version

PTN3392BS/Fx

- BS = HVQFN48 plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; 7x7x0.85 mm SOT619-1
- Fx = Firmware identification option (Fx= 1,2,3, etc and indicates latest firmware version)
- Firmware version reflected on shipping box and reel but not on part symbol
- Firmware options will be identified by periodic Application Sheet updates, not by PCN
- Fx option must be selected at order entry
- Gives customer option of controlling firmware version
DisplayPort-VGA Adapter Roadmap
PTN3372 — DisplayPort to VGA Bridge with 5V Regulator

- **DisplayPort receiver v1.1a**
  - 1-lane / 2-lane 2.7Gb/s / 1.62Gb/s
  - AUX channel, HPD support

- **Output**
  - Analog RGB, HSYNC, VSYNC
  - Up to 240MHz, 8bits color
  - DDC

- **Resolutions**
  - WUXGA: 1920 x 1200, 60Hz, 193MHz clock
  - UXGA: 1600 x 1200, 60Hz, 162MHz clock
  - SXGA (CRT): 1280 x 1024, 80Hz, 135MHz clock
  - SXGA: 1280 x 1024, 60Hz, 108MHz clock
  - XGA: 1024 x 768, 60Hz, 65MHz clock
  - VGA: 640 x 480, 60Hz, 25MHz clock

- Aux channel to i²C DDC channel bridge
- Supports Flash over AUX field upgradability
- 3.3V supply; 0 … 85 °C
- <700mW active; 150mW standby
- No support for HDCP or audio
- HVQFN48, 7x7mm, 0.5mm pitch
- ESD HBM 7kV

**PTN3372 = PTN3392 + Integrated 3.3V to 5V Voltage Reg**
- **Integrated solution for Low-cost DP-VGA Dongle**
- **Lowest system BOM**
- 3.3V to 5V voltage regulator supports 75mA load

### Output
- Analog RGB, HSYNC, VSYNC
- Up to 240MHz, 8bits color
- DDC

### DP configuration | RBR: 1.62 Gbps | HBR: 2.70 Gbps
--- | --- | ---
1 Lane | XGA, SDTV | SXGA, 1080i
2 Lanes | SXGA, 1080i | WUXGA

**Sampling NOW**
Production TBD
PTN3352 — Low-Power DisplayPort to VGA Bridge

- DisplayPort receiver v1.1a
  - 1-lane / 2-lane 2.7Gb/s / 1.62Gb/s
  - AUX channel, HPD support

- Output
  - Analog RGB, HSYNC, VSYNC
  - Up to 240MHz, 8bits color
  - DDC

- Resolutions
  - WUXGA: 1920 x 1200, 60Hz, 193MHz clock
  - UXGA: 1600 x 1200, 60Hz, 162MHz clock
  - SXGA (CRT): 1280 x 1024, 80Hz, 135MHz clock
  - SXGA: 1280 x 1024, 60Hz, 108MHz clock
  - XGA: 1024 x 768, 60Hz, 65MHz clock
  - VGA: 640 x 480, 60Hz, 25MHz clock

- Aux channel to I²C DDC channel bridge
- 1.5V and 3.3V supply; 0 … 85 °C
- Target 400mW active @ 1920 x 1200; 10mW standby
- No support for HDCP or audio
- Support fast link training
- eDP Content Protection mechanisms
  - Support Alternate Framing
  - Support Alternate Scrambler Reset
- HVQFN40, 6x6mm, 0.5mm pitch
- ESD HBM 8kV
- 3.3V HSYNC / VSYNC outputs (min. 3.0V)
- Clock Reference Options
  - Crystal, ceramic resonator, external clock input

Does not support Flash over AUX field upgradability

<table>
<thead>
<tr>
<th>DP configuration</th>
<th>RBR: 1.62 Gbps</th>
<th>HBR: 2.70 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Lane</td>
<td>XGA, SDTV</td>
<td>SXGA, 1080i</td>
</tr>
<tr>
<td>2 Lanes</td>
<td>SXGA, 1080i</td>
<td>WUXGA</td>
</tr>
</tbody>
</table>

In Development

CONFIDENTIAL
NXP PL-Interface Products, 2009
NXP’s DisplayPort Adapter Solutions
# PTN33xx for DisplayPort-DVI and HDMI dongles

<table>
<thead>
<tr>
<th>Feature</th>
<th>PTN3360A</th>
<th>PTN3360B</th>
<th>PTN3361B</th>
<th>PTN3380B</th>
<th>PTN3360D</th>
<th>PTN3381B</th>
<th>PTN3381D</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMDS level shifters</td>
<td>2.5Gb/s</td>
<td>2.5Gb/s</td>
<td>1.65Gb/s</td>
<td>1.65Gb/s</td>
<td>2.5Gb/s (Deep Color HDMI)</td>
<td>1.65Gb/s</td>
<td>2.5Gb/s (Deep Color)</td>
</tr>
<tr>
<td>3.3V to 5V voltage regulator</td>
<td>☒</td>
<td>☒</td>
<td>☒</td>
<td>☑</td>
<td>☒</td>
<td>☑</td>
<td>☑</td>
</tr>
<tr>
<td>DDC level shifter</td>
<td>Pass-gate</td>
<td>Pass-gate</td>
<td>Buffer</td>
<td>Pass-gate</td>
<td>Buffer</td>
<td>Buffer</td>
<td>Buffer</td>
</tr>
<tr>
<td>HPD level shifter</td>
<td>1.1V inverting</td>
<td>3.3V non-inverting</td>
<td>3.3V non-inverting</td>
<td>3.3V non-inverting</td>
<td>3.3V non-inverting</td>
<td>3.3V non-inverting</td>
<td>3.3V non-inverting</td>
</tr>
<tr>
<td>Respond to I²C HDMI dongle detect</td>
<td>-</td>
<td>-</td>
<td>☑ Option pin</td>
<td>-</td>
<td>-</td>
<td>☑ Option pin</td>
<td>☑ Option pin</td>
</tr>
<tr>
<td>Programmable Equalization</td>
<td>☒</td>
<td>☒</td>
<td>☒</td>
<td>☒</td>
<td>☑</td>
<td>☒</td>
<td>☒</td>
</tr>
<tr>
<td>ESD HBM</td>
<td>8kV</td>
<td>8kV</td>
<td>7kV</td>
<td>8kV</td>
<td>6kV</td>
<td>7kV</td>
<td>6kV</td>
</tr>
<tr>
<td>Application</td>
<td>DVI / HDMI on MBD/DVI dongle</td>
<td>DVI / HDMI on MBD/DVI dongle</td>
<td>HDMI dongle</td>
<td>DVI dongle</td>
<td>DVI / HDMI on MBD/DVI dongle</td>
<td>HDMI dongle</td>
<td>HDMI dongle</td>
</tr>
</tbody>
</table>

**In Production**

**Products in Development**

---

**NOTE:** I2C HDMI dongle detect is a mandatory feature for DisplayPort-HDMI dongle
PTN3360B AC-Coupled to DVI/HDMI Level Shifter

**Inputs**
- 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
- 1 HPD from display HPD_Sink to GMCH HPD_Source
- 1 pair for DDC (I²C SCL and SDA)

**Outputs**
- 4 pairs of TMDS outputs - up to 2.5Gb/s per lane
- 1 pair for DDC level shifter
- Non-inverting level-shifting HPD inverter
- 3.3V ± 10% power supply
- Active 35mA typical
- -40 to +85 °C
- ESD 8kV HBM
- HVQFN 48-pin package, 7x7 mm

In Production
PTN3360D AC-Coupled to DVI/HDMI Level Shifter

Inputs
- 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
- 1 HPD from display HPD_Sink to GMCH HPD_Source
- 1 pair for DDC (I2C SCL and SDA)

Outputs
- 4 pairs of TMDS outputs - up to 2.5Gb/s per lane
- Supports HDMI Deep Color at 10bits/color
- 1 pair for DDC level shifter / buffer

Programmable equalizer
Non-inverting level-shifting HPD inverter
3.3V ± 10% power supply
Active 35mA typical
-40 to +85 °C
ESD 6kV HBM
HVQFN 48-pin package, 7x7 mm
PTN3361B AC-Coupled to DVI/HDMI Level Shifter

- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm terminators and bias voltage
  - 1 HPD from display HPD_Sink to north bridge HPD_Source
  - 1 pair for DDC (I²C SCL and SDA)

- **Outputs**
  - 4 pairs of TMDS outputs - Up to 1.65Gb/s per lane
  - 1 pair for DDC buffer and level shifter
  - Optional I²C-based HDMI dongle detect

- Respond to HDMI dongle detect via I²C (option pin)
  - Mandatory feature for DisplayPort-HDMI dongle

- 3.3V ± 10% power supply
- Active current consumption t.b.d.
- -40 to +85 °C
- ESD 8kV HBM (target)
- PTN3361BBS: HVQFN-48, 7x7 mm
- Suitable for DisplayPort-HDMI Dongle
PTN3361B - HDMI Dongle Detect via I²C

- When connected to a DVI dongle or HDMI dongle, how does a multi-standard source determine what display interface to transmit?
  - Pin 13 = HIGH means a dongle is attached
  - Source reads at I²C address 81h
    - If DVI dongle, no response from dongle
    - If HDMI dongle, dongle returns a predetermined character sequence

- PTN3361B supports HDMI dongle detect via I²C
  - Option pin DDET tied LOW for DVI dongle
  - Option pin DDET tied HIGH for HDMI dongle

<table>
<thead>
<tr>
<th>Internal pointer offset</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
<td>44</td>
<td>50</td>
<td>20</td>
<td>48</td>
<td>44</td>
<td>4D</td>
<td>48</td>
<td>20</td>
<td>41</td>
<td>44</td>
<td>41</td>
<td>50</td>
<td>54</td>
<td>4F</td>
<td>62</td>
<td>04</td>
</tr>
</tbody>
</table>

DVI 1.0/HDMI Mode | DisplayPort Pins
---|---
Channel 2 | Main Link Lane 0
Channel 1 | Main Link Lane 1
Channel 0 | Main Link Lane 2
Channel Clock | Main Link Lane 3
DDC Clock | AUX CH+
DDC Data | AUX CH-
DP_PWR | DP_PWR (±3.3V)
Hot Plug Detect | Hot Plug Detect

Cable Adaptor Detect (Optional) Pin 13
CEC (HDMI cable adaptor only) Pin 14
PTN3380B  AC-Coupled to DVI/HDMI Level Shifter & 3.3V/5V Regulator

- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
  - 1 HPD from display HPD_Sink to GMCH HPD_Source
  - 1 pair for DDC (I²C SCL and SDA)

- **Outputs**
  - 4 pairs of TMDS outputs - up to 1.65Gb/s per lane
  - 1 pair for DDC level shifter

- Non-inverting level-shifting HPD inverter
- 3.3V ± 10% power supply
- Active Current TBD
- -40 to +85 °C
- ESD 8 kV HBM (target)
- HWQFN 48-pin package, 7x7 mm
- PTN3380B = PTN3360B + Integrated 3.3V to 5V Voltage Regulator
  - Integrated solution for Low-cost DP-DVI Dongle; Lowest system BOM
  - 3.3V to 5V voltage regulator supports 55mA load

COMPANY CONFIDENTIAL 24
PTN3381B HDMI Level Shifter w/ DDC Buffer & 3.3V/5V Regulator

- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
  - 1 HPD from display HPD_Sink to GMCH HPD_Source
  - 1 pair for DDC (I²C SCL and SDA)

- **Outputs**
  - 4 pairs of TMDS outputs - Up to 1.65Gb/s per lane
  - 1 pair for DDC level shifter
  - Optional I²C-based HDMI dongle detect

- Respond to HDMI dongle detect via I²C (option pin)
  - Mandatory feature for DisplayPort-HDMI dongle

- 3.3V ± 10% power supply
- 0 to +70 °C
- ESD 8kV HBM (target)
- PTN3381BBS: HVQFN-48, 7x7 mm
- PTN3381B = PTN3361B + Integrated 3.3V to 5V Voltage Regulator
  - Integrated solution for Low-cost DP-HDMI Dongle
  - 3.3V to 5V voltage regulator (55mA)
DPDVI Reference Design
NXP DP-DVI dongle with PTN3360B or PTN3360D or PTN3361B or PTN3380B

- Availability: NOW
- Hardware:
  - Hardware ready for both PTN3360B/60D/61B and PTN3380B (stuff option)
  - Form factor optimized as a production-ready dongle
  - Reflects best practices in schematics and layout
  - Reflects best-in-class BOM cost
  - Constitutes a reference design of PTN3360B/D, PTN3361B, PTN3380B

- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC

- Purposes
  1. Customer reference design
  2. PTN3360/3361/3380 interop testing
  3. Trade show demos
DPHDMI Reference Design
NXP DP-HDMI dongle with PTN3361B or PTN3361D or PTN3381D

- Availability: Soon
- Hardware:
  - Hardware ready for both PTN3361B, PTN3361D, and PTN3381B (stuff option)
  - Form factor optimized as a production-ready dongle
  - Reflects best practices in schematics and layout
  - Reflects best-in-class BOM cost
  - Constitutes a reference design of PTN3361B, PTN3361D and PTN3381D

- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC

- Purposes
  1. Customer reference design
  2. PTN3361/3381 interop testing
  3. Trade show demos
PTN3360/1, PTN3380/1 Schedule

PTN3360BBS
✓ PTN3360BBS Production DONE
✓ DP-DVI Reference Design (PTN3360) AVAILABLE
✓ DP-DVI Reference Design Interoperability Tests (PTN3360) AVAILABLE

PTN3361BBS
✓ PTN3361BBS Production DONE
✓ DP-DVI Reference Design (PTN3361) AVAILABLE
✓ DP-DVI Reference Design Interoperability Tests (PTN3361) AVAILABLE
  - DP-HDMI Reference Design (PTN3361) 2H, 2010
  - DP-HDMI Interoperability Tests (PTN3361) 2H, 2010

PTN3360DBS
✓ PTN3360DBS Production DONE

PTN3380BBS
✓ PTN3380BBS Production DONE
✓ DP-DVI Reference Design (PTN3380) AVAILABLE
✓ DP-DVI Reference Design Interoperability Tests (PTN3380) AVAILABLE

PTN3381BBS
✓ PTN3381BBS Sampling AVAILABLE
  - PTN3381BBS Production 2H, 2010
APPENDIX: Firmware Update via Host Flash-over-AUX Feature
# Firmware updater Tested on these PCs

<table>
<thead>
<tr>
<th>Computer</th>
<th>OS</th>
<th>GPU</th>
<th>Driver Version</th>
<th>VBIOS Version</th>
<th>Flash over AUX Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dell Latitude E5400</td>
<td>Vista SP1</td>
<td>Mobile Intel 4 Series Express Chipset</td>
<td>8.15.10.2018</td>
<td>1659</td>
<td>Working</td>
</tr>
<tr>
<td>Dell Dimension 4700</td>
<td>WinXP SP2</td>
<td>NVIDIA GeForce 9400GT</td>
<td>195.62</td>
<td>62.94.4A.00.00</td>
<td>Working</td>
</tr>
<tr>
<td>MacBook Pro</td>
<td>OS X 10.5.6</td>
<td>NVIDIA GeForce 9400M</td>
<td>OS X 10.5.6</td>
<td>OS X 10.5.6</td>
<td>Not available for Mac OS yet</td>
</tr>
<tr>
<td>Lenovo W700</td>
<td>Vista SP1</td>
<td>NVIDIA Quadro FX 2700M</td>
<td>195.62</td>
<td>62.94.45.00.10</td>
<td>Working</td>
</tr>
<tr>
<td>HP ProBook 5310m</td>
<td>WinXP SP3</td>
<td>Mobile Intel 4 Series Express Chipset</td>
<td>6.14.10.2018</td>
<td>1785</td>
<td>Working</td>
</tr>
<tr>
<td>Dell Studio 14z</td>
<td>Vista SP1</td>
<td>NVIDIA GeForce 9400M</td>
<td>195.62</td>
<td>62.79.5B.00.05</td>
<td>Working</td>
</tr>
<tr>
<td>Lenovo 3000H Series</td>
<td>Vista SP1</td>
<td>ATI Radeon HD3470</td>
<td>10.3 (8.01.01.1010)</td>
<td>010.088.000.031</td>
<td>Working</td>
</tr>
<tr>
<td>Intel Calpella</td>
<td>Win7</td>
<td>Intel HD Graphics</td>
<td>8.15.10.2018</td>
<td>1960</td>
<td>Working</td>
</tr>
<tr>
<td>Customer Reference Board (CRB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX: Compliance and EMI Test Results
PTN3392 DisplayPort PHY Compliance Test

- Jitter and height measurement with RBR & HBR (Gain 0 to 7) @ -5°C, 25°C, 85°C
  - @ 2MHz
  - @ 10MHz
  - @ 20MHz
  - @ 100MHz

Input measurement: HBR @ 100MHz

<table>
<thead>
<tr>
<th>Speed</th>
<th>Lane 0</th>
<th>Lane 1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Lane 0</strong></td>
<td>-5 °C</td>
<td>25 °C</td>
</tr>
<tr>
<td>RBR 2 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>RBR 10 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>RBR 20 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>HBR 2 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>HBR 10 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>HBR 20 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>HBR 100 MHz</td>
<td>PASS</td>
<td>PASS</td>
</tr>
</tbody>
</table>

Tektronix AWG Compliance Test Suite

AWG pattern
Amplitude: AWG 700mV + attenuator 10dB

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Jitter Frequency</th>
<th>Number of Bits</th>
<th>Max Number of Bit Errors Allowable</th>
<th>Observation Time (seconds)</th>
<th>Data Rate Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBR</td>
<td>2 MHz</td>
<td>10^12</td>
<td>1000</td>
<td>HBR=370s, RBR=620s</td>
<td>0</td>
</tr>
<tr>
<td>HBR</td>
<td>10 MHz</td>
<td>10^13</td>
<td>100</td>
<td>HBR=37s, RBR=62s</td>
<td>+350ppm</td>
</tr>
<tr>
<td>HBR</td>
<td>20 MHz</td>
<td>10^13</td>
<td>100</td>
<td>HBR=37s, RBR=62s</td>
<td>+350ppm</td>
</tr>
<tr>
<td>HBR</td>
<td>100 MHz</td>
<td>10^11</td>
<td>100</td>
<td>HBR=37s, RBR=62s</td>
<td>0</td>
</tr>
</tbody>
</table>

To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^11 bits at HBR = 370ps/10^11 = 37 seconds)
PTN3392 DP Link Layer Compliance Tests
PTN3392 VSIS v1.2 VGA Compliance Tests

- Resolutions tested
  - VGA 640x480@60Hz, 8 bits per color, 25.175MHz clock
  - SVGA 800x600@60Hz, 8 bits per color, 40MHz clock
  - XGA 1024x768@60Hz, 8 bits per color, 65MHz clock
  - SXGA 1280x1024@60Hz, 8 bits per color, 108MHz clock
  - SXGA 1280x1024@85Hz, 8 bits per color, 135MHz clock
  - UXGA 1600x1200@60Hz, 8 bits per color, 162MHz clock
  - WUXGA 1920x1200@60Hz, 8 bits per color, Reduced Blanking, 154 MHz clock
  - WUXGA 1920x1200@60Hz, 6 bits per color, 193 MHz clock

Setup:
- Tektronix VM6000
- DPVGA4 dongle

Summary:

<table>
<thead>
<tr>
<th></th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>H Sync</td>
<td>PASS</td>
</tr>
<tr>
<td>V Sync</td>
<td>PASS</td>
</tr>
<tr>
<td>Color Bars</td>
<td>PASS</td>
</tr>
<tr>
<td>Ch-Ch Mismatch</td>
<td>PASS</td>
</tr>
<tr>
<td>Ch-Ch Skew</td>
<td>PASS</td>
</tr>
<tr>
<td>Luma Levels</td>
<td>PASS</td>
</tr>
<tr>
<td>Noise Inj Ratio</td>
<td>PASS</td>
</tr>
<tr>
<td>Linearity</td>
<td>PASS</td>
</tr>
<tr>
<td>Video Transient</td>
<td>PASS</td>
</tr>
<tr>
<td>H Sync Jitter</td>
<td>PASS</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VSIS Requirement</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video Noise injection ratio</td>
<td>+/- 2.5% of Max Luminance Voltage</td>
</tr>
<tr>
<td>Video Channel to Video Channel Output Skew</td>
<td>50% of minimum pixel clock period</td>
</tr>
<tr>
<td>Overshoot/Undershoot</td>
<td>+/-12% of step function voltage level over the full voltage range</td>
</tr>
</tbody>
</table>

Video Signals (VSIS Table 2.2)
PTN3392 VGA DAC INL Measurement Update

- Set up: Tektronix VM6000
- DPVGA4 dongle
- Status: Previously failing resolutions NOW PASS
- Datasheet updated to reflect INL of +/-1 LSB

DAC INL previously failing at some resolutions

- Determined that VM6000 has linearity anomalies for given sensitivity and offset settings that impact results
- Sensitivity changed from 96mV/div to 80 mV/div
- Measurement averages set to “3”, waveform averages set to 500 to compensate for oscilloscope noise effects

Measurements retaken with results below. Previously failing resolutions highlighted in dark orange

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Measured INL (LSB)</th>
<th>Previous Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>640x480@60Hz</td>
<td>&lt; +/- 1</td>
<td>Fail</td>
</tr>
<tr>
<td>800x600@60Hz</td>
<td>&lt; +/- 1</td>
<td>Pass</td>
</tr>
<tr>
<td>1024x768@60Hz</td>
<td>&lt; +/- 1</td>
<td>Pass</td>
</tr>
<tr>
<td>1280x1024@60Hz</td>
<td>&lt; +/- 1</td>
<td>Pass</td>
</tr>
<tr>
<td>1600x1200@60Hz</td>
<td>&lt; +/- 1</td>
<td>Fail</td>
</tr>
<tr>
<td>1920x1200@60RB</td>
<td>&lt; +/- 1</td>
<td>Fail</td>
</tr>
<tr>
<td>1920x1200@60Hz</td>
<td>&lt; +/- 1</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Table 12. DAC characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_{\text{ref}}(\text{DAC})</td>
<td>DAC resolution</td>
<td>-</td>
<td>8</td>
<td>bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f_{\text{clk}}</td>
<td>clock frequency</td>
<td>-</td>
<td>240</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Δ_{\text{I}_{\text{D}}}(\text{DAC})</td>
<td>DAC-to-DAC output current matching</td>
<td>-</td>
<td>4</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td>integral non-linearity</td>
<td>-1</td>
<td>+0.5</td>
<td>+1</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>DNL</td>
<td>differential non-linearity</td>
<td>-1</td>
<td>+1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{\text{O}}(\text{comp})</td>
<td>DAC output voltage compliance</td>
<td>0</td>
<td>1.25</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{\text{O}}</td>
<td>DAC output capacitance</td>
<td>-</td>
<td>3.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>α_{\text{c}(\text{DAC})}</td>
<td>DAC crosstalk between DAC outputs</td>
<td>-</td>
<td>-54</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**DPVGA4 EMI Test Results and Findings**

**EMI Chamber Tests**

- **Test Setup**
  - DPVGA4 Prototype Dongle with PTN3392
  - Dell Latitude E6500 with power supply and mouse
  - Scrolling “H” pattern
  - Philips Brilliance 200P LCD monitor
  - Resolutions Tested
    - 800 x 600; 1600 x 1200, 1280 x 1024

- **EMI Test Findings**
  - PASS CISPR22B without metal shielding (however, without the desired 3-6dB margin)
  - PI-filter is indeed not necessary for EMI reasons
    - However, RGB filtering needed to pass VSIS

**Semi-Anechoic Chamber**

Recommend metal tape around VGA connector or metal cage
### DPVGA4 IEC61000-4-2 ESD Tests

<table>
<thead>
<tr>
<th>Test Performed</th>
<th>Test date</th>
<th>Level</th>
<th>Criteria/Result</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD – Enclosure</td>
<td>2010/02/19</td>
<td>4</td>
<td>B / Pass</td>
<td>Notes Deviations</td>
</tr>
</tbody>
</table>

Pass without external ESD Protection Devices!
### DPVGA4 IEC61000-4-2 ESD Tests

#### Indirect Discharges (to Coupling Planes)

<table>
<thead>
<tr>
<th></th>
<th>Positive Polarity (kV)</th>
<th>Negative Polarity (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Contact Mode</strong></td>
<td>Level 1</td>
<td>Level 2</td>
</tr>
<tr>
<td><strong>VCP located 10cm from the front, rear, left, and right sides of the EUT</strong></td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td><strong>HCP located 10cm from the front, rear, left, and right sides of the EUT</strong></td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

#### Direct Discharges (to the EUT)

<table>
<thead>
<tr>
<th></th>
<th>Positive Polarity (kV)</th>
<th>Negative Polarity (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Contact Mode</strong></td>
<td>Level 1</td>
<td>Level 2</td>
</tr>
<tr>
<td><strong>VGA shell</strong></td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td><strong>Display Port shell</strong></td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

#### Air Discharge Mode

<table>
<thead>
<tr>
<th></th>
<th>Positive Polarity (kV)</th>
<th>Negative Polarity (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Contact Mode</strong></td>
<td>Level 1</td>
<td>Level 2</td>
</tr>
<tr>
<td><strong>VGA shell</strong></td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td><strong>Display Port shell</strong></td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note 1:** An “X” indicates that the EUT continued to operate as intended.

**Note 2:** ND: No discharges was possible due to lack of discharge path to ground from test point.

- HCP: Horizontal Coupling Plane,
- VCP: Vertical Coupling Plane.

**Note 3:** Image disappeared but returned to normal by itself. Criterion B.

**Note 4:** 10 positive and 10 negative discharges applied to each side of EUT.
APPENDIX: Interoperability Test Suites
## DisplayPort Sources

<table>
<thead>
<tr>
<th>Computer Model</th>
<th>Type</th>
<th>Graphics Card</th>
<th>OS</th>
<th>Graphics Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dell Latitude E5400</td>
<td>Laptop</td>
<td>Mobile Intel 4 Series Express Chipset</td>
<td>Vista SP1</td>
<td>8.15.10.2018</td>
</tr>
<tr>
<td>Dell Dimension 4700</td>
<td>Laptop</td>
<td>NVIDIA GeForce 9400GT</td>
<td>WinXP SP2</td>
<td>195.62</td>
</tr>
<tr>
<td>MacBook Pro</td>
<td>Laptop</td>
<td>NVIDIA GeForce 9400M</td>
<td>OS X 10.5.6</td>
<td>OS X 10.5.6</td>
</tr>
<tr>
<td>Lenovo W700</td>
<td>Laptop</td>
<td>NVIDIA Quadro FX 2700M</td>
<td>Vista SP1</td>
<td>195.62</td>
</tr>
<tr>
<td>HP ProBook 5310m</td>
<td>Laptop</td>
<td>Mobile Intel 4 Series Express Chipset</td>
<td>WinXP SP3</td>
<td></td>
</tr>
<tr>
<td>Dell Studio 14z</td>
<td>Laptop</td>
<td>NVIDIA GeForce 9400M</td>
<td>Vista SP1</td>
<td>195.62</td>
</tr>
<tr>
<td>Lenovo 3000H Series</td>
<td>Desktop</td>
<td>ATI Radeon HD3470</td>
<td>Vista SP1</td>
<td>10.3 (8.01.01.1010)</td>
</tr>
<tr>
<td>Calpella CRB</td>
<td>Laptop</td>
<td>Intel HD Graphics</td>
<td>Win7</td>
<td>8.15.10.2018</td>
</tr>
<tr>
<td>Lenovo 3000H Series</td>
<td>Desktop</td>
<td>ATI Radeon HD5750</td>
<td>Vista SP1</td>
<td>10.1 (8.01.01.994)</td>
</tr>
</tbody>
</table>

## Sinks (Monitors used w/ VGA)

<table>
<thead>
<tr>
<th>Monitor Model</th>
<th>Highest Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHILIPS 190B</td>
<td>1280x1024</td>
</tr>
<tr>
<td>ACER X213W</td>
<td>1680x1050</td>
</tr>
<tr>
<td>DELL 1905FP</td>
<td>1280x1024</td>
</tr>
<tr>
<td>DELL 2408WFP</td>
<td>1920x1200</td>
</tr>
<tr>
<td>DELL 1908FP</td>
<td>1280x1024</td>
</tr>
<tr>
<td>SAMSUNG LT4065F</td>
<td>1920x1080</td>
</tr>
</tbody>
</table>

## VGA Cables Used

<table>
<thead>
<tr>
<th>Cable Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>6ft</td>
</tr>
<tr>
<td>15ft</td>
</tr>
<tr>
<td>50ft</td>
</tr>
<tr>
<td>100ft</td>
</tr>
</tbody>
</table>
# Interoperability Test Matrix

<table>
<thead>
<tr>
<th>Sink</th>
<th>Source</th>
<th>Firmware</th>
<th>Test Name</th>
<th>Cable Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>860×660 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>860×660 @ 72</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>860×660 @ 75</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1024×756 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1024×768 @ 70</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1024×768 @ 75</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280×960 @ 60Hz</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280×960 @ 75Hz</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1360×768 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1600×1200 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1920×1200 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Shutdown</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Restart</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Hibernate</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>HDP</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Standby</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Timeout</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Single</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Clone</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Extended</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Resolution Fig of Mer</td>
<td>ft</td>
</tr>
<tr>
<td>2408WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Overall Fig of Merit</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>800×660 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>800×660 @ 72</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>960×660 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>960×660 @ 75</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1024×768 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1152×864 @ 75Hz</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1280×768 @ 60Hz</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1920×1200 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1152×864 @ 75Hz</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1280×768 @ 60</td>
<td>ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVIDIA FX2700</td>
<td>1.07</td>
<td>1024×756 @ 70</td>
<td>ft</td>
</tr>
</tbody>
</table>

## Company Confidential
June 22, 2010

Interface Products / Ho Wai Wong-Lam
Resolution Figure of Merit

Definition: Resolution Figure of Merit =
Average score of all resolution tests
- Each source-to-sink combination may have a unique # and list of resolutions
- Each test score has equal weight

- Each test gets a score on a scale of 1 to 10.
  - 1 = failed test, not user fixable
    - E.g. Permanent Blinking, blanking, flashing
  - 5 = fixable or occasional flaw
    - E.g. by changing resolution image may be restored
  - 10 = pass
    - Perfect image

- Interpretation Guide
  - 10 = Perfect (our goal)
  - Score ≥ 9.9 acceptable
  - 1 = Total Failure

<table>
<thead>
<tr>
<th>Sink</th>
<th>Source</th>
<th>Firmware</th>
<th>Test Name</th>
<th>Cable Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>800x600 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>800x600 @ 72</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>800x600 @ 75</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1024x768 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280x960 @ 75</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280x960 @ 75</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280x1024 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280x1024 @ 75</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1280x1024 @ 75</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1360x768 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1600x1200 @ 60</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>1920x1200 @ 90</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Shutdown</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Restart</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Hibernate</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>HD</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Standby</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Timeout</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Single</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Clone</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Extended</td>
<td>6ft</td>
</tr>
<tr>
<td>240WFP</td>
<td>ATI HD3650</td>
<td>1.07</td>
<td>Resolution Fig of Merit</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>800x600 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>800x600 @ 72</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>960x600 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>960x600 @ 75</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>1024x768 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>1152x864 @ 50</td>
<td>6ft</td>
</tr>
<tr>
<td>1905FP</td>
<td>Lenovo NVidia FX2700</td>
<td>1.07</td>
<td>1280x768 @ 50</td>
<td>6ft</td>
</tr>
</tbody>
</table>
Overall Figure of Merit

Definition: Overall Figure of Merit =
Average score of all interop tests
• Each source-to-sink combination may have a unique # and list of all tests
• Each test score has equal weight
• Tests include Hotplug, EDID, Clone, Primary, etc.. AND all resolution tests

– Each test gets a score on a scale of 1 to 10.
  • 1 = permanently failed test, not user fixable
    – E.g. Permanent Hot-plug fail, simple primary no image
  • 2 = largely failed test
    – E.g. 7 out of 8 Hot-plugs fail
  • 5 = fixable or occasional flaw
    – E.g. @ the native resolution the test fails, multiple Hot-plugs fixes error
  • 8 = fixable or occasional flaw, minor
    – E.g. @ mid-range resolution the test fails, occasional random test fail
  • 10 = pass
    – Perfect image
**Interop Status**

- **Interoperability**
  - Windows (Dell) / NVIDIA GeForce 9400GT
  - Windows (Dell)/NVIDIA Quadro NVS 160M
  - Mac OS X (Apple) / NVIDIA GeForce 9400M
  - Windows (Dell) / Intel GMA4500 chipset
  - Windows (Lenovo) / ATI Radeon HD5750
  - Windows (Lenovo) / NVIDIA Quadro FX 2700M
  - Windows (Dell) / NVIDIA GeForce 9400M
  - Windows (HP) / Intel GMA4500 chipset
  - Windows (Intel Customer Reference Board) / Intel HD Graphics

---

**Good interoperability**

- Good Interoperability
- Good Interoperability
- Good Interoperability
- Good Interoperability
- Good Interoperability
- Good Interoperability
- Good Interoperability
- Good Interoperability

---

<table>
<thead>
<tr>
<th>Issue requires attention for root cause analysis in PTN3392</th>
<th>No issues found in this category</th>
</tr>
</thead>
<tbody>
<tr>
<td>Medium severity issue with PTN3392</td>
<td>No issues found in this category</td>
</tr>
<tr>
<td>Issue unrelated to PTN3392</td>
<td>Some issues found in this category</td>
</tr>
<tr>
<td>This is likely due to the source/sink combination</td>
<td></td>
</tr>
<tr>
<td>Minority issue with PTN3392</td>
<td>A limited number of issues found in this category</td>
</tr>
<tr>
<td>(User recoverable usually with auto-adjust button on the monitor)</td>
<td></td>
</tr>
</tbody>
</table>
Thank you!